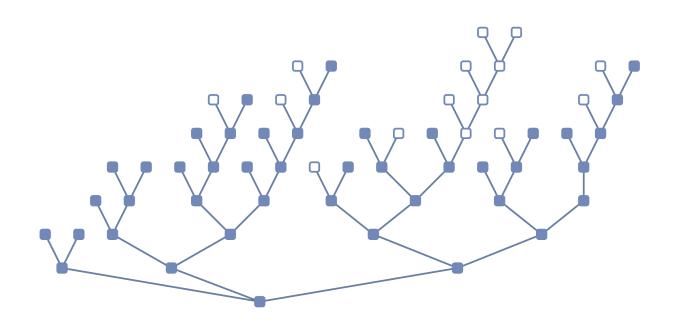
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Hensel CPU Arithmetic Logic Units

Circuit Design for Exact Computing with 2-adic Arithmetic

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1 2-Adic Arithmetic Logic

The Hensel CPU is being developed by SciSci Research and Future Computing to realize an exact computing capability to replace floating-point computation. Unlike floating point numbers, which are approximations of numbers in \mathbb{R} , the Hensel CPU performs exact arithmetic in \mathbb{Q}_2 , or, moreover, on finite encodings of 2-adic numbers. Arithmetic operations are executed in the Hensel CPU processor by 2-adic arithmetic logic units (2AALUs). At the circuit level, 2AALU operations on FC-3-2025-encoded operands (i.e., finite encodings of coefficients of 2-adic expansions) are performed via combinational logic by Boolean logic gates. Indeed, coefficient values in 2-adic expansions are either 0 or 1, as, in turn, are the entries in FC-3-2025 encodings of operands. Thus, exact computing in \mathbb{Q}_2 with the Hensel CPU is compatible with extant MOSFET technology; 2AALUs compute in bits with normal logic gates. Given herein is a circuit-level description of 2AALU arithmetic.

1.1 Setup

We will consider a Hensel CPU model more expansive than that seen in the forthcoming Virtual Hensel demonstration. Here, we will consider a Hensel capable of storing operands up to 30 bits in length, where the respective maximal R_{FC} , L_{FC} , and T_{FC} lengths are 10 bits each. This Hensel can perform arithmetic operations on operands up to 15 bits in length, where the respective maximal R_{FC} , L_{FC} , and T_{FC} lengths are 5 bits each. According to the Hensel architecture, such a CPU would have a cluster of 1024 processor registers for distributed loadstore of operands. As previously discussed, a commercial-grade Hensel will have a large bit-width, larger than that considered herein. A key point to underscore in this report is, even for high bit widths, the relative simplicity by which 2-adic operands can be subject to arithmetic.

This report will describe binary additive operations, i.e., addition as performed on input operand pairs. Arithmetic proceeds as follows. We begin with operands $\chi^{\mathfrak{d}}\left(\mathsf{FC}(\mathsf{q})\right)$ and $\chi^{\mathfrak{d}}\left(\mathsf{FC}(\mathsf{p})\right)$ and an arithmetic operation $\mu:=\Upsilon^{\mathsf{post}}\left(\Upsilon\left(-\right)\right)$. Here, Υ is the main arithmetic step, involving addition on $\chi^{\mathfrak{d}}$ entries that do not require carrying 1 entries to extra "digit" places. This is the most computationally demanding procedure, i.e., it employs the most gates. In our case, Υ acts on $\chi^{\mathfrak{d}}\left(\mathsf{FC}(\mathsf{p})\right)$ and $\chi^{\mathfrak{d}}\left(\mathsf{FC}(\mathsf{q})\right)$, which are each five bits in length, giving an output that is also five bits in length. Next, Υ^{post} is applied to $\Upsilon\left(-\right)$, and supplies extra-"digit" 1 values as needed.

The combinational logic for the above procedure is written out, and circuit diagrams are provided. Additionally, it is explained how FC-2-2025 instructions, which have previously been mentioned in the Virtual Hensel and load-store reports, are computed. (It's nothing more than a simple XOR gate computation.)

For a given pair of operands FC(q) and FC(p), the above procedures are performed for 1) $\chi_{(*,-,-)}^{\mathfrak{d}}(\mathsf{FC}(\mathsf{p}))$ and $\chi_{(*,-,-)}^{\mathfrak{d}}(\mathsf{FC}(\mathsf{q}))$, 2) $\chi^{\mathfrak{d}}_{(-,*,-)}(FC(p))$ and $\chi^{\mathfrak{d}}_{(-,*,-)}(FC(q))$, and 3) $\chi^{\flat}_{(-,-,*)}$ (FC(p)) and $\chi^{\flat}_{(-,-,*)}$ (FC(q)). All entries are fed from right to left; thus, in the case of $\chi^{\mathfrak{d}}_{(-,-,*)}\left(\mathsf{FC}(\mathsf{p})\right)$ and $\chi^{\mathfrak{d}}_{(-,-,*)}\left(\mathsf{FC}(\mathsf{q})\right)$ (i.e., T_{FC}), the entries are reversed, beginning with the right-most pair $\left({}^{T}a_{5}^{p},{}^{T}a_{5}^{q}\right)$ and ending with the left-most pair $({}^{\mathsf{T}}\mathsf{a}_1^\mathsf{p}, {}^{\mathsf{T}}\mathsf{a}_1^\mathsf{q})$. In the case of $\chi^{\mathfrak{d}}_{(*,-,-)}(\mathsf{FC}(\mathsf{p}))$ and $\chi^{\mathfrak{d}}_{(*,-,-)}(\mathsf{FC}(\mathsf{q}))$ (i.e., R_{FC}), as well as $\chi^{\mathfrak{d}}_{(-,*,-)}$ (FC(p)) and $\chi^{\mathfrak{d}}_{(-,*,-)}$ (FC(q)) (i.e., L_{FC}), addition begins with (Ra_1^p, Ra_1^q) or (La_1^p, La_1^q) . Here, we will simply write (a_1^p, a_1^q) to refer to the first entry for a general pair, with it understood that this is $({}^{T}a_{5}^{p}, {}^{T}a_{5}^{q}), ({}^{R}a_{1}^{p}, {}^{R}a_{1}^{q}),$ or $(L_{a_1}^p, L_{a_1}^q)$. The same follows accordingly that (a_5^p,a_5^q) can be $\left(^Ta_1^p,^Ta_1^q\right)$, $\left(^Ra_5^p,^Ra_5^q\right)$, or (La_5^p, La_5^q) . The output will be written from left to right, with the (a_1^p, a_1^q) output furthest to the left and the (a_5^p, a_5^q) furthest to the right.

2 Combinational Logic

2.1 Length-5 Addition

We begin with Υ procedures, each of which yields an output ω_i ($1 \le i \le 5$). The first output entry, ω_1 , is obtained thusly:

 $Xor[a_1^p, a_1^q]$

The Υ procedure for ω_2 is as follows:

$$\begin{split} &\text{Or}[\text{Xor}[\text{And}[\text{And}[a_{1}^{p}, a_{1}^{q}], \text{Nor}[a_{2}^{p}, a_{2}^{q}]], \\ &\text{And}[\text{Nand}[a_{1}^{p}, a_{1}^{q}], \text{Xor}[a_{2}^{p}, a_{2}^{q}]]], \\ &\text{And}[\text{And}[a_{1}^{p}, a_{1}^{q}], \text{And}[a_{2}^{p}, a_{2}^{q}]]] \end{split}$$

The Υ procedure for ω_3 is as follows:

 $Or[Or[And[And[a_1^p, a_1^q], Or[a_2^p, a_2^q]],$ $Nor[a_3^p, a_3^q]$, And $[And[a_2^p, a_2^q]$, $Nor[a_3^p, a_3^q]], Or[And[Nor[a_2^p, a_2^q]],$ $Xor[a_3^p, a_3^q]], And[And[Nand[a_1^p, a_1^q]],$ Nand $[a_2^p, a_2^q]$, Xor $[a_3^p, a_3^q]$]], $And[And[a_2^p, a_2^q], And[a_3^p, a_3^q]]],$ And $[And [And [a_1^p, a_1^q], Or [a_2^p, a_2^q]],$ And $[a_3^p, a_3^q]$, Nor $[a_4^p, a_4^q]$], And [And [Xor $[a_4^p, a_4^q]$, And $[a_3^p, a_3^q]$], $Nor[a_5^p, a_5^q]]$, And [And [And [And [And [a₁^p, a₁^q]]], $Or[a_2^p, a_2^q]], And[a_3^p, a_3^q]],$ And $[a_4^p, a_4^q]$, Nor $[a_5^p, a_5^q]$], $Not[And[And[And[Nand[a_1^p, a_1^q],$ $Xor[a_2^p, a_2^q]], And[a_3^p, a_3^q]],$ $Xor[a_4^p, a_4^q]]]$, $Not[And[And[Nor[a_2^p, a_2^q]]]$ And $[a_3^p, a_3^q]$, Xor $[a_4^p, a_4^q]$

The Υ procedure for ω_4 is as follows:

And[And[And[Xor[Or[Or[And [And [And [a_1^p, a_1^q], Or [a_2^p, a_2^q]], $Or[a_3^p, a_3^q]], Nor[a_4^p, a_4^q]],$ And [And [a_2^p, a_2^q], $Or[a_3^p, a_3^q]$], $Nor[a_4^p, a_4^q]]$, And $[And[a_3^p, a_3^q]$, $Nor[a_4^p, a_4^q]]$, $Nand[a_1^p, a_1^q], Nand[a_2^p, a_2^q]],$ Nand[a_{3}^{p}, a_{3}^{q}]], Xor[a_{4}^{p}, a_{4}^{q}]], And $[Nor[a_3^p, a_3^q], Xor[a_4^p, a_4^q]]],$ And $[And[Nor[a_2^p, a_2^q], Nand[a_3^p, a_3^q]],$ $Xor[a_4^p, a_4^q]], And[Nor[a_3^p, a_3^q],$ $Xor[a_4^p, a_4^q]], And[And[a_3^p, a_3^q],$ And $[a_4^p, a_4^q]$, And $[And [Xor [a_3^p, a_3^q]]$, And $[a_4^p, a_4^q]$, Nor $[a_5^p, a_5^q]$]], $Not[And[And[And[Xor[a_1^p, a_1^q],$ $Xor[a_2^p, a_2^q]], Xor[a_3^p, a_3^q]],$ $And[a_4^p, a_4^q]]]$, $Not[And[And[Nor[a_2^p, a_2^q]]]$ $Xor[a_3^p, a_3^q]], And[a_4^p, a_4^q]]]],$ $Not[And[And[Nor[a_1^p, a_1^q], Xor[a_2^p, a_2^q]],$ $Xor[a_3^p, a_3^q]], And[a_4^p, a_4^q]]]]$

The Υ procedure for ω_5 is as follows:

Or[Or[Or[Or[Or[And $[And [And [And [a_1^p, a_1^q],$ $Or[a_2^p, a_2^q]], Or[a_3^p, a_3^q]],$ $Or[a_4^p, a_4^q]], Nor[a_5^p, a_5^q]],$ And $[And [And [a_2^p, a_2^q], Or [a_3^p, a_3^q]],$ $Or[a_4^p, a_4^q]], Nor[a_5^p, a_5^q]]],$ And [And [a_3^p, a_3^q], Or [a_4^p, a_4^q]], $Nor[a_5^p, a_5^q]]],$ And $[And [a_4^p, a_4^q], Nor [a_5^p, a_5^q]]],$ $Or[Or[And[And[And[And[Nand[a_1^p, a_1^q],$ $Nand[a_2^p, a_2^q]], Nand[a_3^p, a_3^q]],$ Nand $[a_4^p, a_4^q]$, Xor $[a_5^p, a_5^q]$, And $[Nor[a_4^p, a_4^q], Xor[a_5^p, a_5^q]]]$ And $[And [a_4^p, a_4^q], And [a_5^p, a_5^q]]]]$ And $[And[Nor[a_3^p, a_3^q], Nand[a_4^p, a_4^q]], Xor[a_5^p, a_5^q]]],$ And $[And [Nor[a_2^p, a_2^q], Nand[a_3^p, a_3^q]],$ $Nand[a_4^p, a_4^q]], Xor[a_5^p, a_5^q]]]$

Length-5 Addition COMBINATIONAL LOGIC

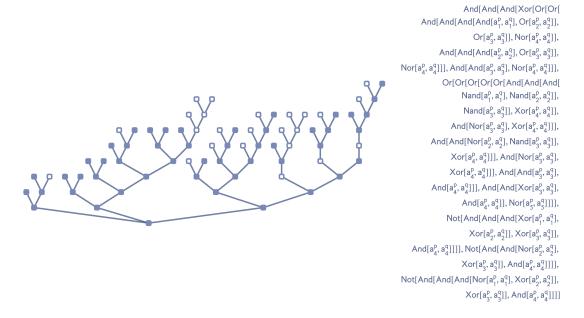


Figure 1: Illustration of correspondence between the combinational procedure for ω_4 and the graph structure of its circuit. (Inputs are omitted from graph.) In this case, $a_1^p = True$, $a_1^q = False$, $a_2^p = True$, $a_3^p = False$, $a_3^p = False$, $a_4^p = False$, $a_4^p = False$, $a_4^p = False$, $a_5^p = True$, and $a_5^p = False$.

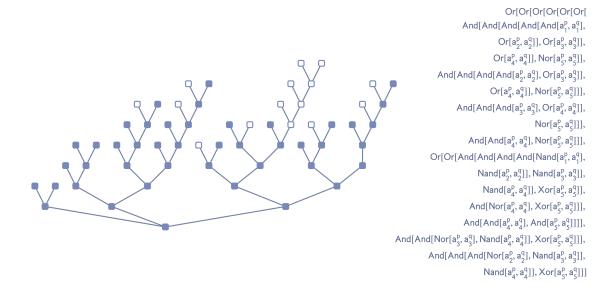


Figure 2: Illustration of correspondence between the combinational procedure for ω_5 and the graph structure of its circuit. (Inputs are omitted from graph.) In this case, $a_1^p = \text{True}$, $a_1^q = \text{False}$, $a_2^p = \text{True}$, $a_2^q = \text{False}$, $a_3^q = \text{False}$, $a_4^q = \text{False}$, $a_4^q = \text{False}$, $a_4^p = \text{False}$, $a_5^p = \text{True}$, and $a_5^q = \text{True}$.